

2. Adding a ferrite bead (L2) allows the rectifier to turn off by momentarily blocking the current through the MOSFET when it tries to change direction. This action eliminates the large reverse-current spike, so a typical efficiency gain of 7% over the nonsynchronous design is achieved.

the current through the MOSFET when it tries to change direction, allowing the rectifier to be properly commutated. This results in a typical

efficiency improvement of 7% at currents of a few hundred milliamps. The low-resistance beads are available in small surface-mount packages. Diode

D1 provides a current path at the beginning of the rectifier conduction cycle, because the bead also delays the current through Q1 at turn-on.

Circle 521

Active Cancellation Of A Pot's Wiper Resistance

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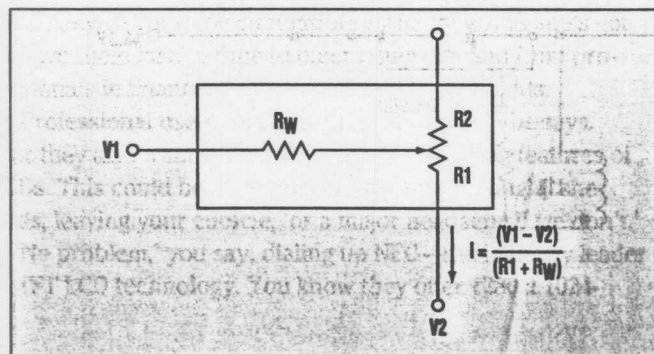
Although we almost always call them "potentiometers," many (if not most) adjustable resistance devices actually end up being used as two-terminal variable resistors

(rheostats). In actuality, the term "potentiometer" means a three-terminal variable voltage divider.

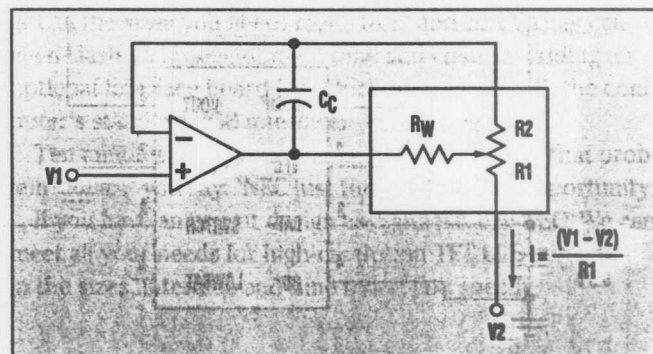
Unfortunately, when used as variable resistors, pots (whether electro-

mechanical or electronic) suffer from a number of non-idealities that can thoroughly bust an error budget. Chief culprits among these parasites is the "wiper resistance."

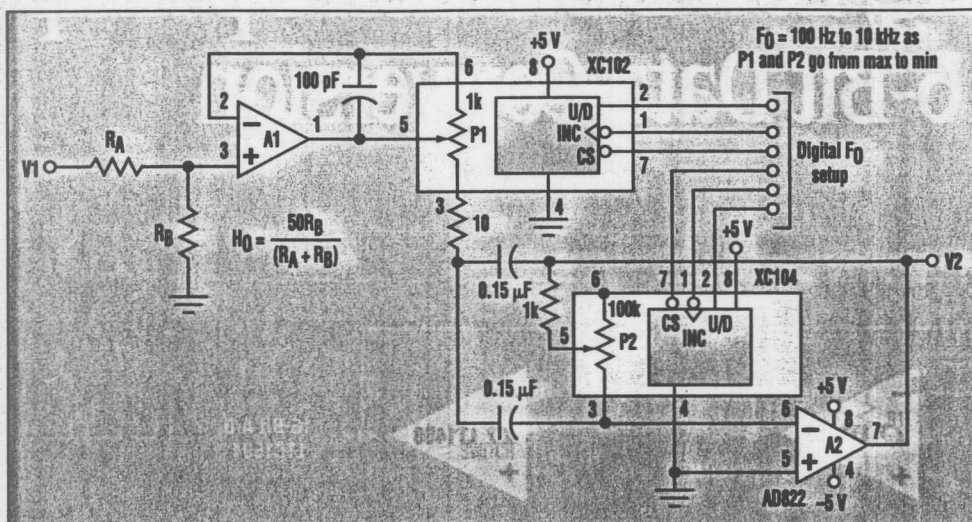
Wiper resistance arises in electro-mechanical pots because they consist of a stationary resistance element over which a sliding contact (wiper) moves to set the desired resistance. Perversely, the contact point between wiper and resistance element itself inevitably makes an undesired non-zero contribution (R_W in figure 1) to the total resistance ($R_1 + R_W$). The effective resistance of the pot can therefore never be adjusted all the way to zero



1. Uncompensated wiper resistance (R_W) can cause serious instabilities due to time, temperature, and life-cycle wearout mechanisms.



2. This arrangement effectively blots out wiper-resistance-related difficulties using electromechanical or electronic potentiometers.



3. The new topology is put to good use in a wide-range ($f_0 = 100 \text{ Hz}$ to 10 kHz) Q-of-5, digitally tunable bandpass filter application. DCP P2 does not need this trick due to its larger 2500:1 R_W -to-element ratio.

but instead has a minimum value directly related to R_W . What's worse, R_W is strongly influenced by surface phenomena lurking in the mechanical interface between wiper and resistance element. This makes it seriously unstable against time, temperature, and life-cycle wearout mechanisms.

Electronic (digitally controlled) potentiometers (DCPs), on the other hand, escape the contact resistance problems of the mechanical pot. However, they must contend instead with the relatively large R_{ON} resistances (usually tens of ohms) of the FET switches that implement the multiplexer, which substitutes for the mechanical pot's wiper.

While FETs don't wear out and get noisy like mechanical wipers, the FETs' R_{ON} temperature coefficients approach $3000 \text{ ppm}/^\circ\text{C}$ —five to ten

times worse than typical resistance elements. Therefore, even relatively small R_W contributions to total circuit resistance may significantly degrade circuit stability. Take, for example, the Xicor XC102 digitally controlled pot. Its 1k resistance element has a tempco of $\pm 600 \text{ ppm}/^\circ\text{C}$ max, and the setting resolution is 10Ω . R_W is typically 40Ω . For resistance settings of 200Ω or less, the overall resistance tempco is dominated by R_W . In addition, because R_W can range as high as 100Ω , the resistance setting accuracy is at the mercy of R_W for settings below 500Ω . Not a pretty picture.

Figure 2 illustrates a way to effectively blot out these R_W -related difficulties. It relies on the fact that, since the resistance component R_2 conducts only negligible (op amp bias) currents, the voltage at the amplifiers (-) input

is essentially the same as the voltage at the R_1 - R_2 node and therefore equal to $(I \cdot R_1 + V_2)$ independent of R_W . Consequently, when the op amp forces the R_1 - R_2 node to V_1 (as it must to maintain input balance), I is forced to accurately equal $(V_1 - V_2)/R_1$, and thus the R_W effects vanish. Optional frequency compensation in the form of C_C will sometimes be needed to avoid op-amp feedback instability resulting from phase shift in R_2 .

Figure 3 shows the new topology put to good use in a wide-range ($f_0 = 100 \text{ Hz}$ to 10 kHz) Q-of-5, digitally tunable bandpass filter. DCP P2 (100k) isn't bothered much by R_W effects, due to

its typical 2500:1 R_W -to-element resistance ratio. Therefore, it wouldn't benefit from Figure 2's trickery. But DCP P1's performance would be compromised significantly (due to its 25:1 ratio) at low-resistance (high-frequency) settings if nothing were done to cancel its R_W . A1 does that while simultaneously buffering the R_A - R_B voltage divider, the adjustment of which can set passband gain anywhere from 0 to 50.

The incremental (up/down) digital interface of P1 and P2 makes this filter ideal for frequency-tracking applications. Such applications have a phase-sensitive quadrature detector/comparator combination that can be used to generate the up/down direction control signal for both DCPs. As a result, it's possible to implement a feedback loop that will automatically converge on optimum tuning.

Circle 522

Better Linearity For Frequency-To-Voltage Converters

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In many applications, such as frequency-locked-loop circuits or tachometers, a dc voltage propor-

tional to an input frequency is required. Some special ICs are specifically designed for a highly linear frequency-to-

voltage conversion (e.g., the AD650 from Analog Devices). However, these devices aren't commonly available, compared to simple CMOS 4000 series or 74HC series ICs, and their price is typically much higher. On the other hand, if an inexpensive one-shot such as a 74HC423 or a CD4528 is used for frequency-to-voltage conversion, the linearity is generally unsatisfactory.

Adding a very simple RC network improves the linearity between dc output voltage U_{DC} and input frequency f by least one decade. The figure illustrates a standard frequency-to-voltage conversion arrangement